Yeabsira Hawaz

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Education

Massachusetts Institute of Technology — Cambridge, MA
M.S. in Electrical Engineering and Computer Science — *Anticipated 2027*
B.S. in Electrical Engineering and Computer Science; Minor in Musical Technology — *Class of 2026*

Coursework: Grad Digital Systems/RFSoC, Accelerated GPU Programming, Digital Systems Lab, Semiconductors, Microcomputer Project Lab, Constructive Computer Architecture **GPA:** 4.7/5.0

Experience

zeroRISC — Boston, MA
Hardware Engineering Intern — *06/2025 – 08/2025*
- Designed and developed a AXI IP for OpenTitan—the first open-source silicon root of trust—transitioning its bus architecture from TileLink-UL to AXI
- Developed SystemVerilog implementations of a TileLink-UL to AXI4 bridge and an AXI CSR interface bridge, enabling the OpenTitan chip to interface with peripherals via AXI
- Wrote Verilator C++ test benches and validated designs on a Xilinx VCU118 FPGA board with various Xilinx AXI IP cores, and verified against existing tape-out UVM DV

MIT Computer Science & Artificial Intelligence Laboratory — Cambridge, MA
Undergraduate Researcher, Computer Architecture Group — *01/2024-Present*
- Architected and implemented a 2D-torus Network-on-Chip for a sparse linear algebra accelerator, achieving 400 MHz synthesis on an AMD Alveo U55C
- Implemented dual virtual channels and a two-stage pipeline, reducing average packet latency to 17 cycles—1.3× faster than comparable mesh NoCs under heavy traffic.
- Validated the design via cycle-accurate simulation and hardware integration, passing stress-tests with 16×16 networks under 150K+ message workloads.

Johns Hopkins Applied Physics Lab — Laurel, MD
Software Engineering Intern, Robotics Group — *06/2023-08/2023*
- Developed a novel methodology and platform for unit testing behavior tree-based MAVROS drones
- Wrote integration tests to emulate the preplanned actions of a MAVROS operated drone, decreasing time spent on workbench testing the drone after each update

Projects

Holoforge: A Gesture Controlled 3D Model Viewer — 10/2024-06/2025
- Designed and implemented a camera-controlled 3D model viewer on a Xilinx FPGA, with a custom graphics pipeline (pre-proc, shader, rasterizer) and AXI-backed DDR3 framebuffer
- Developed centroid tracking using an Adafruit camera to control scene view in real time
- Built a custom AXI stacker to optimize out-of-order writes to DDR3 via the MIG, enabling double-buffered rendering at 360×180 resolution

Jazzy Dude — 03/2025-05/2025
- Designed and implemented a jazz-based instrument synthesizer on a PSoC 5LP in C, generating saxophone and piano sounds using custom ADSR envelopes and phase accumulators.
- Programmed real-time playback and transposition of pre-programmed jazz standards, enabling dynamic key and tempo adjustments entirely in firmware.

SuperScalar Processor — 05/2024
- Designed and implemented a two-wide superscalar RISC-V processor in Bluespec
- Synthesized and ran the processor on a Urbana FPGA Board, trained against the MNIST Dataset 15% faster than a base line scalar pipelined processor

Technical Skills

Languages: SystemVerilog, Bluespec, C/C++, CUDA, RISC-V Assembly, Python, ROS, x86 Assembly
Developer Tools: Xilinx Vivado, Verdi, Verilator, Vivado ILA, TCL, GIT, Linux, Bash Scripting
Hardware/Design: FPGA Development, ZYNQ, AXI, UART, TileLink, Digital Circuit Design, Embedded Systems, Memory Management, Timing Analysis

Teaching

MIT EECS — 01/2025 – Present
Lab Assistant — *Cambridge, MA*
- Digital Systems Laboratory (6.2050) FA2025: Held office hours and assisted students with FPGA-based labs with topics such as SPI, UART, and HDMI
- Computation Structures (6.1910) SP2025: Held office hours and assisted students in architecture labs with topics such as caching, pipelined processors, and operating systems